DETAILED ACTION

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with George Neuner on 10/9/2008.

The application has been amended as follows:

In claim 5, please delete "a control part that executes control to alternately repeat provide a logarithmic operation first period..." and replace it with "a control part that executes control to provide a logarithmic operation first period...".

Allowable Subject Matter

Claims 1-8 are allowed.

The following is an examiner's statement of reasons for allowance:

Re claims 1-4, the prior art fails to teach or suggest: "A solid-state imaging device in which a photodiode and a first transistor are provided in series between a ground and a drain in each pixel, and a signal corresponding to a current or an electric charge generated in the photodiode according to an optical input is outputted from a detection node located between the photodiode and the first transistor, comprising: a control part that executes control to provide **a logarithmic operation first period** during which a photoelectric conversion signal logarithmically converted by setting a gate voltage of the first transistor to a first level is obtained followed by **a linear operation second period** during which a linear photoelectric conversion signal is obtained by setting the gate voltage of the first transistor to a second level, **and to repeatedly alternate a logarithmic operation period and a linear operation period**".

Re claims 5-8, the prior art fails to teach or suggest, "A solid-state imaging device in which a photodiode and a first transistor are provided in series between a ground and a drain in each pixel, and a signal corresponding to a current or an electric charge generated in the photodiode according to an optical input is outputted from a detection node located between the photodiode and the first transistor, comprising: a control part that executes control to alternately repeat a logarithmic operation first period during which a photoelectric conversion signal logarithmically converted by setting a gate voltage of the first transistor to a first level is obtained and followed by a linear operation second period during which a linear photoelectric conversion signal is obtained by setting the gate voltage of the first transistor to a second level, and to repeatedly

alternate a logarithmic operation period and a linear operation period, wherein the control part executes control so as to alternately repeat the logarithmic operation period and the linear operation period every frame, **read a potential of the detection node as a linear type signal immediately before a transition from the linear operation period to the logarithmic operation period, and read the potential of the detection node as a logarithmic signal in the logarithmic operation period after a lapse of a certain period after the transition to the logarithmic operation period**".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Watanabe (US 7,012,238) discloses an amplification-type solid-state image pickup device incorporating a plurality of arrayed pixels with an amplification function. The information regarding amplification within a solid-state image sensor is relevant material.

Fossum et al. (US 2003/0193597) discloses a single substrate camera device with a CMOS image sensor. The information regarding amplification within a solid-state image sensor is relevant material.

Doering et al. (US 2004/0196398) discloses a CMOS image sensor and method for operating a CMOS image sensor with increased dynamic range. The information regarding amplification within a solid-state image sensor is relevant material.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached at **(571) 272-7372**. The fax phone number for submitting all Official communications is **(571) 273-7300**. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at (571) 273-7312.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kelly L. Jerabek/

Examiner, Art Unit 2622

/Lin Ye/

Supervisory Patent Examiner, Art Unit 2622